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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,506	03/26/2004	Pavel Horsky	BGC.0005US (A2261-US)	8179

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,506	HORSKY ET AL.	
	Examiner	Art Unit	
	Jean B Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohya (US patent Number 5,745,064) in view of Vogt et al. (US patent Number 5,105,193).

3. Regarding claims 1 and 11 Ohya discloses a two-dimensional matrix decoder and method for a digital-to-analog converter (figs. 5, 6A, 6B) comprising an array of current cells (437e, fig. 5) the cells having a current source means (451, figs. 6A, 6B; col 11, lines 40, 41, 46, 47) or a current divider means and a switching means (452, fig. 6A, 6B), all cells being activatable in a pre-determined sequence, the matrix decoder (figs. 5, 6A, 6B) [the decoders shown in fig. 5] comprising a selection means (435e, fig. 5)[the decoders in figs. 5 select the cells] outputting a first selection signal for selecting a cell, matrix logic unit (450, fig. 6A, 6B) associated with each cell for generating a control signal suitable for controlling the switching means of that cell for switching current from the current source means or current divider means of that cell to at least one of a first node or a second node, the control signal being generated depending on the first selection signal and the cell state signal (col 11, lines 28 – 33, 52 – 65). Ohya does not specifically disclose a two-dimensional matrix decoder for a digital-to-analog

converter wherein the matrix decoder comprises a cell state signaling means outputting a cell state signal determining whether a cell comes before or after a selected cell in a predetermined sequence. However, in a related field, discloses a DAC (figs. 1, 2) that comprises array of current cells (4) in which the state of the cells are determined (col 2, lines 27 – 37)[the matrix 4 in fig. 1 comprises a plurality of cells in which the latch 14 maintains current source 8 in its existing state; the current source being part of the current cell implies that its state may be ON/OFF or a cell may come before or after a selected cell in a predetermined sequence]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ohya's system with that of Vogt et al.'s system in order to operate current sources in response to a digital coded input signal to produce a total analog output current of an appropriate magnitude.

4. Regarding claims 2, 12, Ohya discloses a matrix decoder and method (figs. 5, 6A, 6B), wherein the selection means comprises a first decoder (431a, fig. 5) outputting a first selection signal for selecting a first set of cells, and a second decoder (431b, fig. 5) outputting a second selection signal for selecting a second set of cells. the first and second set of cells having the selected cell in common (figs. 5, 6A, 6B).

5. Regarding claims 3, 13, Ohya discloses a matrix decoder and method (figs. 5, 6A, 6B) wherein the first decoder (431a) is a row decoder and the first set of cells is a row of cells and the second decoder (431b) is a column decoder and the second set of cells is a column of cells.

6. Regarding claim 4, Ohya discloses a matrix decoder (figs. 5, 6A, 6B) wherein the first node is an output node of the digital-to-analog converter and the second node is a ground node or dummy node of the digital-to-analog converter (fig. 5, 6A, 6B).

7. Regarding claim 5, Ohya discloses a matrix decoder (figs. 5, 6A, 6B) wherein the first node (433) is an output node of the digital-to-analog converter and the second node (434) is a ground node or dummy node of the digital-to-analog converter (figs. 5, 6A, 6B).

8. Regarding claims 6, 14, Ohya discloses a matrix decoder and method (figs. 5, 6A, 6B) wherein the pre-determined sequence is such that a sequence of cells starts in the middle of the matrix and expands from the middle to the sides of the matrix (fig. 5).

9. Regarding claims 7, 15, Ohya discloses a matrix decoder and method (figs. 5, 6A, 6B) wherein the pre-determined sequence is such that a sequence of cells starts in the middle of the matrix and expands from the middle to the sides of the matrix (fig. 5).

10. Regarding claims 8, 16, Ohya discloses a matrix decoder and method (figs. 5, 6A, 6B) wherein the control signal generated by the matrix logic unit (450, figs. 6A, 6B) is suitable for controlling the switching means of that cell for switching current to either of a first, a second or a third node (figs. 5, 6A, 6B)[note the switching means in figs. 6A, 6B by the control signal of the control logic 450 that activates transistor 452].

11. Regarding claims 9, 17, Ohya discloses a matrix decoder and method (figs. 5, 6A, 6B) wherein the control signal generated by the matrix logic unit (450, figs. 6A, 6B) is suitable for controlling the switching means of that cell for switching current to either

of a first, a second or a third node (figs. 5, 6A, 6B)[note the switching means in figs. 6A, 6B by the control signal of the control logic 450 that activates transistor 452].

12. Regarding claim 10, Ohya discloses a digital-to-analog converter (fig. 5) comprising: an array of current cells (437, fig. 5), all cells being activatable in a pre-determined sequence (fig. 5), a current source means (451, figs. 6A, 6B) or current divider means and a switching means (452, figs. 6A, 6B) , and a matrix decoder (435e, fig. 5).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Hareyama (US Patent Number 4,393,370) discloses a DAC using matrix of current sources.

15. Park (US patent Number 5,623,264) discloses a video DAC.

16. Yoshida et al. (US patent Number 5,760,725) discloses a current cell type DAC.

17. Ogawara (EP 0 482 842) discloses a DAC unit with improved linearity.

18. Nakamura et al. (US patent Number 5,327,134) discloses a DAC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
November 18, 2004